IN THE CLAIMS

1. (Currently amended) A memory system having a plurality of memory chips, comprising:

an address clock driver to generate an address clock signal in response to a current chip signal and an address count-up signal, wherein the current chip signal activates a currently selected chip from the plurality of memory chips;

a counter to generate an address including a chip information and a sector information, wherein the chip information identifies the chip from the plurality of memory chips; and

a control circuit to generate the address count-up signal with reference to that the sector information corresponds to a sector to be erased.

2. (Original) The memory system as set forth in claim 1, wherein the control circuit has a chip selection information to check the sector information when the chip selection information is identical to the chip information of the counter.

3. (Original) The memory system as set forth in claim 1, wherein an output of the address clock driver is conditioned at a high impedance state when the chip selection information is different from the chip information of the counter.

4. (Original) The memory system as set forth in claim 2, wherein the chip selection information is established by a hard-coded option.

5. (Original) The memory system as set forth in claim 1, wherein the counter generates addresses in sequence.

6. (Original) The memory system as set forth in claim 5, wherein the chip information of the counter corresponds to a most significant address bit.

7. (Currently amended) A memory system having a plurality of memory chips, comprising:

a memory cell array constructed of a plurality of sectors;

a register circuit to store a loaded sector information about a sector to be erased;

an address clock driver to generate address clock signals contemporaneously for the chips in response to a current chip signal and an address count-up signal;

a counter to generate an address including a chip information and a sector information, wherein the chip information identifies the chip active from the plurality of memory chips;

a control circuit to generate the address count-up signal and an erase enable signal with reference to that the loaded sector information corresponds to the sector information of the counter; and

a core driver to carry out an erase operation for a corresponding sector in response to the erase enable signal.

8. (Original) The memory system as set forth in claim 7, wherein the control circuit has a chip selection information to check the sector information when the chip selection information is identical to the chip information of the counter.

9. (Original) The memory system as set forth in claim 7, wherein an output of the address clock driver is conditioned at a high impedance state when the chip selection information is different from the chip information of the counter.

10. (Original) The memory system as set forth in one of claims 8 and 9, wherein the chip selection information is established by a hard-coded option.

11. (Original) The memory system as set forth in claim 7, wherein the counter generates addresses in sequence.

12. (Original) The memory system as set forth in claim 11, wherein the chip information of the counter corresponds to a most significant address bit.

13. (Currently amended) A memory system having a plurality of memory chips, comprising:

a first bus to transfer control signals;

a second bus to transfer address and data signals; and

a plurality of memory chips connected to the first and second buses, wherein each memory chip comprises:

a memory cell array constructed of a plurality of sectors;

a register circuit to store a loaded sector information about a sector to be erased;

an address clock driver to generate address clock signals contemporaneously for the chips in response to a current chip signal and an address count-up signal;

a counter to generate an address including a chip information and a sector information, wherein the chip information identifies the chip from the plurality of chips;

a control circuit to generate the address count-up signal and an erase enable signal with reference to that the loaded sector information corresponds to the sector information of the counter; and

a core driver to carry out an erase operation for a corresponding sector in response to the erase enable signal.

14. (Original) The memory system as set forth in claim 13, wherein the control circuit has a chip selection information to check the sector information when the chip selection information is identical to the chip information of the counter.

15. (Original) The memory system as set forth in claim 13, wherein an output of the address clock driver is conditioned at a high impedance state when the chip selection information is different from the chip information of the counter.

16. (Original) The memory system as set forth in one of claims 14 and 15, wherein the chip selection information is established by a hard-coded option.

17. (Original) The memory system as set forth in claim 13, wherein the counter generates addresses in sequence.

18. (Original) The memory system as set forth in claim 17, wherein the chip information of the counter corresponds to a most significant address bit.

19. (Currently amended) A method of erasing multi-sectors in a multi-chip package including a counter, a control circuit, and a register circuit, the method comprising:

initializing an address of the counter;

determining whether a chip information of the counter is identical to a chip selection information of the control circuit, wherein the chip information identifies chip from a plurality of chips;

determining whether a sector information of the counter is identical to a loaded sector information of the register circuit when the chip information of the counter is identical to the chip selection information of the control circuit;

erasing a sector corresponding to the loaded sector information when the sector information of the counter is identical to the loaded sector information; and

terminating the multi-sector erase operation when an erased sector is the last sector.

20. (Original) The method as set forth in claim 19, further comprising, when the chip information is different from the chip selection information, incrementing the address if a currently counted address is irrelevant to the last sector while terminating the multi-sector erase operation when a currently counted address is relevant to the last sector.

21. (Original) The method as set forth in claim 19, further comprising incrementing the address when the erased sector is irrelevant to the last sector.